WHAT IS CLAIMED IS:

1. An integrated circuit comprising:

a plurality of computational elements including a plurality of arithmetic nodes, a plurality of bit-manipulation nodes, a plurality of finite state machine nodes, and a plurality of input/output nodes;

a first and a second processing node each having a core processor based on a common architecture;

a first memory associated with said first processing node;

a second memory associated with said second processing node;

a first node wrapper for coupling said core processor of said first processing node to said first memory and to said computational elements;

a second node wrapper for coupling said core processor of said second processing node to said second memory and to said computational elements; and

means for interconnecting said computational elements and said first and second processing nodes to define a selected task to achieve a desired functionality.

2. The integrated circuit of claim 1 further comprising means for temporally adapting said second node and said computational elements to perform a selected function.

3. The integrated circuit of claim 2 wherein said temporal means further comprises executable code defining said selected function stored in at least said first memory.

4. The integrated circuit of claim 3 wherein said executable code is downloaded from the Internet by said first processing node.

5. The integrated circuit of claim 4 wherein said executable code comprises operating system code.

6. The integrated circuit of claim 5 wherein said first processing node initiates the temporal adaptation of said computational elements and said second processing node to perform said selected function.

7. The integrated circuit of claim 1 wherein said computational elements include a plurality of arithmetic nodes, a plurality of bit-manipulation nodes and a plurality of finite state machine nodes.

8. The integrated circuit of claim 1 further comprises a plurality of said second processing nodes each of which is coupled to said first processing node and computational elements by said interconnecting means.

9. An adaptive computing engine comprising:

a controller node having:

a core processor for executing operating system code;

a memory for storing operating system executable code;

means for transferring operating system executable code and data from said memory to said core processor;

a plurality of computational elements adapted to perform a selected function at least one of said computational elements having:

a RISC processor for executing code;

a memory for storing executable code;

means for transferring executable code and data from said memory to said RISC processor; and

a temporal interconnecting matrix coupling said controller node to said plurality of computational elements to perform a user selected function.

10. The adaptive computing engine of claim 9 wherein said controller node further comprises a configuration register, said configuration register containing a bit for determining whether said controller node functions as a controller or as a RISC processor.

11. The adaptive computing engine of claim 10 wherein said configuration register bit protects a portion of memory from access by said computational elements when set.

12. The adaptive computing engine of claim 10 further comprising a protected portion of memory accessible only to said controller node.

13. The adaptive computing engine of claim 9 wherein said controller node further comprises:

a node wrapper having:

a data distributor for receiving an input stream from an external source, said input stream having configuration information and executable code;

a hardware task manager for receiving configuration information from said data distributor;

a DMA engine for receiving data and executable code from said data distributor;

a controller for providing said node wrapper access a set of registers associated with said core processor;

an interrupt controller for detecting interrupt conditions from said node wrapper and internally; and

a JTAG port associated with a debug register for debugging erroneous operation of said controller node.

14. An adaptive computing engine having a plurality of computational elements and a temporal interconnecting matrix for connecting said computational elements, said adaptive computing engine comprising:

a controller node for adapting said computational elements in response to perform a selected function, said controller node having:

a core processor for executing operating system code;

a memory for storing operating system executable code;

means for transferring operating system executable code and data from said memory to said core processor;

a set of registers associated with said core processor;

a node wrapper, coupled to said core processor, for receiving an input stream from an external source, said input stream having configuration information and executable code and passing said information to said core processor; and

means for accessing said set of registers;

an interrupt controller for detecting interrupt conditions from said node wrapper and internally.

15. The adaptive computing engine of claim 14 further comprising means for accessing said core processor and said memory to debug error conditions.

16. The adaptive computing engine of claim 14 further comprising means for handling node-to-node communication.

17. The adaptive computing engine of claim 14 further comprising executable code for controlling the temporal adaptation of said computation elements in response to configuration information.

18. The adaptive computing engine of claim 17 further comprising means for controlling the initiation of operation of said computational element upon reset or power on.

19. The adaptive computing engine of claim 18 further comprising:

a programmable scalar node having:

a core processor for executing instructions;

an instruction memory for storing said instructions;

a data memory;

means for transferring instructions from instructions memory to said core processor and for transferring data to said core processor from said data memory;

a set of registers associated with said core processor;

a node wrapper, coupled to said core processor, for receiving an input stream from controller node, said input stream having configuration information; and

means for accessing said set of registers;

an interrupt controller for detecting internal interrupt conditions.

20. The adaptive computing engine of claim 19 further comprising:

a data cache; and

an instruction cache.

21. The adaptive computing engine of claim 20 further comprising a memory arbitration unit for managing access to said data memory and said instruction memory.

22. The adaptive computing engine of claim 14 further comprising means for minimizing power consumption.